

ESTIMATION AND CORRECTION OF GAIN MISMATCH AND TIMING ERROR IN TIME-INTERLEAVED ADCs BASED ON DFT

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Abstract

Time-interleaved analog-to-digital converter (ADC) architecture is crucial to increase the maximum sample rate. However, offset mismatch, gain mismatch, and timing error between time-interleaved channels degrade the performance of time-interleaved ADCs. This paper focuses on the gain mismatch and timing error. Techniques based on Discrete Fourier Transform (DFT) for estimating and correcting gain mismatch and timing error in an M-channel ADC are depicted. Numerical simulations are used to verify the proposed estimation and correction algorithm.

Keywords: correction, estimation, gain mismatch, time-interleaved analog-to-digital converter, timing error.

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1. Introduction

In hybrid-signal systems with analog inputs, analog-to-digital conversion is a key function that enables digital processing of samples of the analog signal. However, the sample rates of the analog-to-digital converters (ADCs) often limit the digital signal processing (DSP) systems operating on analog inputs. Time-interleaved ADC architecture with more than one ADC is a well-known technique that can be used to increase the maximum sample rate [1–17]. In such architecture, a fast ADC is obtained by combining slower ADCs operating in parallel. Ideally, the slow ADCs should have the same offset, gain and should sample the signal with uniformly-spaced timing phases in time. However, the performance of time-interleaved ADCs is sensitive to offset and gain mismatches as well as the timing phase errors between the interleaved channels [4, 9], so calibration is necessary. The calibration of these mismatches can be finished by tuning the operation of the parallel ADCs in the analog domain, but it is difficult to accomplish without bringing some new noise. So it is preferable to perform the calibration directly in the digital domain.

Calibration of mismatches between channels requires both estimation and correction of mismatch errors. Digital foreground calibration can be used to remove the mismatches with a known input. In [18], an FFT-based method to evaluate and compensate offset and gain errors in time-interleaved ADC system was proposed with a known sinusoidal input. The timing errors can be extracted from the images in the output spectrum caused by using discrete Fourier transform (DFT) when a known sinusoidal input is applied [6]. A ramp signal can also be used to measure timing errors between the channels [5]. Foreground calibration is easy to implement in practice, but requires a known calibration signal, which means that the operation of the ADC must be stopped during calibration. A blind timing error estimation method was presented in [10] and verified on measurements in [2]. In [14], a digital background calibration method was proposed to calibrate the offset and gain mismatch as well as the timing error. Digital background calibration does not interrupt the conversion of

the input, but its implementation is more complex than the foreground calibration, consuming more time and resources.

This paper focuses on the estimation and correction of gain mismatch and timing error, and the estimation and correction are operated in the foreground. With a known sinusoidal input, the gain and timing errors can be estimated and corrected based on DFT of ADC output. Instead of calculating the DFT of the overall output, the DFT of individual ADC output is used to estimate the gain mismatch and timing error parameters. Explicitly, the magnitude of the individual DFT is used to estimate the gain mismatch, and the timing error is estimated by extracting the phase of an individual DFT. So the algorithm presented in this paper is computationally efficient and can calibrate the gain and timing errors accurately.

The rest of this paper is divided into four sections. Section 2 reviews time-interleaved ADCs and their limitations. Section 3 presents a method to estimate and correct the gain and timing errors. Then, the simulation results are given in Section 4. Finally, conclusions are drawn in Section 5.

2. Time-interleaved ADC architecture

Fig. 1 shows a simplified block diagram of an M-channel time-interleaved ADC. It contains M channels in parallel and a digital multiplexer at the output. Each channel consists of a sub-ADC, and each channel has the same sample period of MT_s and the difference between the sample instants of the adjacent channels is T_s , where T_s denotes the overall sample period. So each channel operates at the overall sample rate $f_s = 1/T_s$ divided by M . An analog input signal is sequentially sampled and digitized by sub-ADCs of the individual channels and the digitized outputs from the M channels are then multiplexed by the digital multiplexer to generate a final ADC digital output. An advantage of this interleaving architecture is that the overall sample rate increases by a factor of M without adopting some new technology. However, the performance of time-interleaved ADC is sensitive to mismatches between the channels.

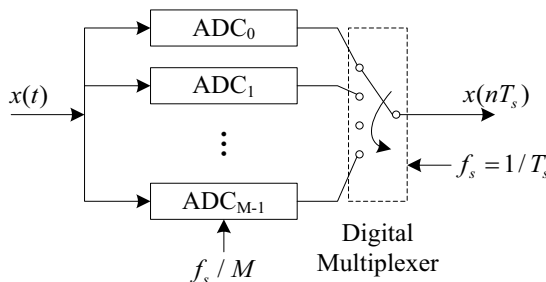


Fig. 1. Block diagram of the M-channel time-interleaved ADC architecture.

Fig. 2 shows a detailed model block diagram of an M-channel time-interleaved ADC with offset mismatch, gain mismatch and timing error. The gain and offset mismatch parameters are denoted g_i and o_i , $i = 0, 1, \dots, M - 1$, respectively, and T_i denotes the sample instants of the i th ADC, and

$$T_i = kMT_s + iT_s + \delta_i T_s, \tag{1}$$

where δ_i denotes the relative timing error. Notation Q_i denotes the quantization function of each channel and $x_i(n)$ denotes the quantized output. If the mismatch errors between different

ADC channels are important and their effect is not negligible when compared with ADC quantization error, they must be calibrated by adopting appropriate algorithms [6]. In this paper, the effect of mismatch errors is assumed to be more significant than the effect of quantization error, so the quantization error is neglected during the derivation of the calibration algorithm in this paper.

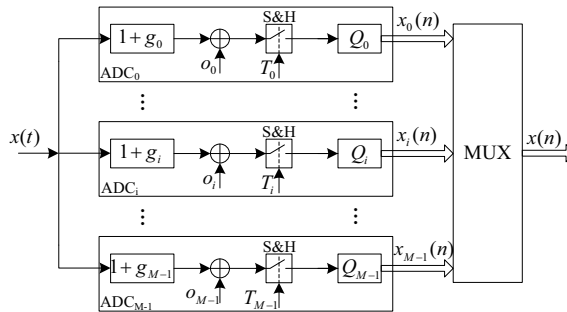


Fig. 2. Model block diagram of the M-channel time-interleaved ADC with offset, gain and timing mismatch errors [18].

With a sinusoidal input, the images in the output spectrum caused by the mismatch errors have been explicitly discussed in [4, 9]. With input signal frequency f_0 , the gain and timing errors cause images at the frequencies

$$f_{noise} = \frac{i}{M} f_s \pm f_0, \quad i = 0, 1, \dots, M - 1, \quad (2)$$

where f_s is the overall sample frequency. The offset error causes images at the frequencies

$$f_{noise} = \frac{i}{M} f_s, \quad i = 0, 1, \dots, M - 1. \quad (3)$$

The timing-error-induced image magnitudes are approximately proportional to the relative timing error δ_i as well as the input frequency f_0 , while the image magnitudes caused by offset and gain mismatch only depend on the corresponding error parameters, i.e. o_i and g_i , respectively [4].

All of these mismatch errors increase the noise floor of the ADC, degrading the system performance. It is therefore important to remove the mismatch errors. Because the offset error calibration is simple and easy to implement, the next section will focus on the calibration method of the gain and timing errors.

3. Gain and timing error calibration

3.1. Problem description

The offset error can be easily calibrated by firstly averaging the ADC output and then subtracting the average value from the ADC output, so this section will analyze the calibration method for the gain and timing errors.

It is assumed that the input signal $x(t)$ is strictly bandlimited to π/T_s by certain external filter [11]. Therefore, the Nyquist sampling criterion with an effective sample frequency of f_s without aliasing is fulfilled, and the continuous-time Fourier transform of $x(t)$,

$$X(j\Omega) = \int_{-\infty}^{\infty} x(t) e^{-j\Omega t} dt, \quad (4)$$

is zero for $|\Omega| > \pi / T_s$. Then, $x(t)$ can be reconstructed exactly from its samples $x(n) = x(nT_s)$.

Instead of using a single ADC to sample the signal, M time-interleaved ADCs with sample period MT_s and relative sample phase offset T_s are employed. However, due to the relative timing error δ_i in (1), the actual sample phase offset between the neighbouring ADCs will deviate somewhat from T_s .

The M -channel time-interleaved ADC is ideal if the M gain mismatch parameters g_i are zero or the same, and so are the M timing error parameters δ_i . In order to estimate and then correct these errors, we choose the first ADC as the reference with the gain and timing error parameters $g_0 = 0$ and $\delta_0 = 0$, respectively. Due to the channel mismatches, the samples obtained at the outputs of the M sample channels can be expressed by

$$x_i(n) = (1 + g_i)x(nMT_s + iT_s + \delta_iT_s), \tag{5}$$

where $i = 0, 1, \dots, M - 1$, and the multiplexed output $x(n)$ is given by

$$x(n) = x_{\lfloor n/M \rfloor}, \tag{6}$$

where $\lfloor \cdot \rfloor$ denotes the downward rounding operation.

Fig. 3 is the analysis filter bank model of the M -channel time-interleaved ADC. In this model, the ADCs are supposed to be ideal, and both of the gain and timing errors are included in the channel frequency responses $H_i(j\Omega)$, where $|\Omega| < \pi / T_s$. The input signal $x(t)$ is filtered by $H_i(j\Omega)$ and then sampled by an ADC, and all of the ADCs operate simultaneously. The frequency response $H_i(j\Omega)$ of each channel is written as

$$H_i(j\Omega) = (1 + g_i)e^{j\Omega T_s(i + \delta_i)}. \tag{7}$$

The frequency response of the reference channel is $H_0(j\Omega) = 1$ due to $g_0 = \delta_0 = 0$. Equation (7) shows that the channel frequency response $H_i(j\Omega)$ introduces gain mismatch and fractional-sample-time delay to the input signal, thus yielding the damaging image frequencies in the overall output spectrum.

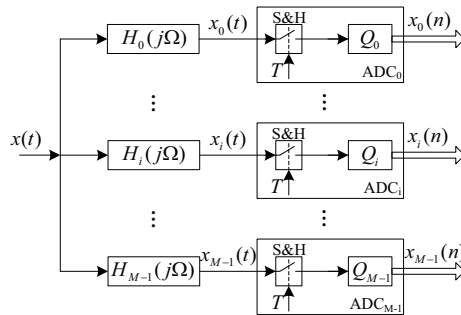


Fig. 3. Analog analysis filter bank model of the M -channel time-interleaved ADC.

3.2. Gain and timing error estimation

The gain and timing error estimation algorithm presented in this paper is based on the DFT. This algorithm needs a known sinusoidal signal as the test input to finish the error parameter estimation and needs not to multiplex the M ADC output to form a higher-speed data stream.

In section 3.1, we have chosen the first ADC as the reference with the gain and timing error parameters $g_0 = 0$ and $\delta_0 = 0$, respectively. Consequently, the gain mismatch error of the i th channel ($i = 1, \dots, M-1$) can be estimated by utilizing the DFT magnitude ratio between the i th channel and the reference channel, and the DFT phase difference between the i th channel and the reference channel can be used to estimate the timing mismatch error of the i th channel.

Let input $x(t)$ be a sinusoidal signal with unit amplitude, frequency f_0 and phase θ , i.e.

$$x(t) = \sin(2\pi f_0 t + \theta), \quad (8)$$

where $f_0 < f_s / 2$. As shown in Fig. 3, $x_i(t)$ is the output of the i th analysis filter $H_i(j\Omega)$. Containing the gain and timing errors introduced by $H_i(j\Omega)$, $x_i(t)$ can be represented by

$$x_i(t) = (1 + g_i) \sin(2\pi f_0 t + 2\pi f_0 (i + \delta_i) T_s + \theta). \quad (9)$$

The frequency response of the reference channel is $H_0(j\Omega) = 1$, so $x_0(t) = x(t)$.

After being sampled-and-held and quantized, the output $x_i(n)$ is given by

$$x_i(n) = (1 + g_i) \sin(2\pi f_0 n M T_s + 2\pi f_0 (i + \delta_i) T_s + \theta). \quad (10)$$

Equation (10) shows that in the analysis filter bank model, all the ADCs sample simultaneously with the same sample rate, i.e. the sample instant $T = n M T_s$.

Let $X_i(e^{j\omega})$ represent the DFT of $x_i(n)$, and $X_i(e^{j\omega})$ can be expressed by

$$X_i(e^{j\omega}) = \frac{(1 + g_i)}{j} \pi [\delta(\omega - 2\pi f_0 n M T_s - 2\pi f_0 (i + \delta_i) T_s - \theta) - \delta(\omega + 2\pi f_0 n M T_s + 2\pi f_0 (i + \delta_i) T_s + \theta)] \quad (11)$$

Considering only the positive frequency or the negative one, the gain mismatch and timing error of the i th channel ($i = 1, \dots, M-1$) can be easily calculated by

$$g_i = \frac{|X_i(f_0)|}{|X_0(f_0)|} - 1, \quad (12)$$

and

$$\begin{aligned} \delta_i &= \frac{\Delta\Phi_i}{2\pi f_0 T_s} - i \\ &= \frac{\Phi_i(f_0) - \Phi_0(f_0)}{2\pi f_0 T_s} - i \end{aligned} \quad (13)$$

In (12) and (13), $|X_k(f_0)|$ and $\Phi_k(f_0)$ represents the magnitude and phase associated with the frequency f_0 in DFT sequence of the i th ADC output.

The sample rate of each ADC is f_s / M , and it is possible that the input frequency f_0 is higher than f_s / M . So aliasing in each ADC cannot be avoided in each ADC if $f_0 > f_s / M$, making the implementation of an estimation algorithm difficult in practice. We restrict the test input frequency f_0 to the following range

$$f_0 \in [0, f_s / M]. \quad (14)$$

Moreover, not all of the frequency value between 0 and f_s / M can be used to estimate the error parameters accurately. As f_0 approaches 0 or f_s / M , the sampled output of each ADC is nearly a DC signal, degrading the accuracy of the estimation algorithm. On the other hand, if f_0 varies towards the Nyquist frequency of each ADC, or $f_s / 2M$, the oversampling factor

$$r = \frac{f_s}{Mf_0}, \tag{15}$$

varies towards 1, resulting in the increasing loss of information in the original signal. A big estimate error appears when f_0 equals 0, $f_s / 2M$ or f_s / M , so (14) can be modified to

$$f_0 \in (0, \frac{f_s}{2M}) \cup (\frac{f_s}{2M}, \frac{f_s}{M}). \tag{16}$$

Based on the above-mentioned theoretical analysis, now we discuss how to estimate the gain and timing errors from the M L-point DFT sequences, where L denotes the DFT length of each ADC output and L must be an integer power of 2. Let $M_i(l)$ and $P_i(l)$ denote the magnitude and phase sequences of the L-point DFT $X_i(e^{j\omega})$, respectively, where $l = 0, 1, \dots, L-1$, and l_0 be the component index associated with the input frequency f_0 in the sequences $M_i(l)$ and $P_i(l)$ of each ADC. The relationship between l_0 and f_0 can be described by

$$l_0 = [Mf_0L / f_s], \tag{17}$$

where $[\]$ represents the rounding operation. The gain mismatch and timing error of the i th channel, i.e. g_i and δ_i are given by

$$g_i = \frac{M_i(l_0)}{M_0(l_0)} - 1, \tag{18}$$

and

$$\delta_i = \frac{P_i(l_0) - P_0(l_0)}{2\pi f_0 T_s} - i. \tag{19}$$

Based on (10) and due to the timing error, the theoretical phase difference between the i th channel and the reference one is

$$\begin{aligned} \Delta\Phi_i &= \Phi_i(f_0) - \Phi_0(f_0) \\ &= 2\pi f_0 (i + \delta_i) T_s. \end{aligned} \tag{20}$$

The absolute value of term δ_i in (20) is much smaller than 1, or $|\delta_i| \ll 1$, so $|\Delta\Phi_i| < 2\pi i / M$. In practice, if $|P_i(l_0) - P_0(l_0)|$ in (19) is bigger than $2\pi i / M$, it will result in wrong estimates, so proper phase compensation $2\pi m$ needs to be subtracted from $P_i(l_0) - P_0(l_0)$ to ensure $|P_i(l_0) - P_0(l_0)| < 2\pi i / M$, where $m \in Z$.

3.3. Gain and timing error correction

With the estimates in (18) and (19), we rewrite the channel frequency response (7) as

$$H_i(j\Omega) = (1 + g_i) e^{j\Omega T_s (i + \delta_i)}. \tag{21}$$

In this paper, we adopt a simple method to correct the gain and timing errors between the channels. The calibration diagram is shown in Fig. 4, where $H'_i(e^{j\omega})$ is the calibration filter with the expression

$$H'_i(e^{j\omega}) = \frac{1}{1 + g_i} e^{-j\omega\delta_i}. \tag{22}$$

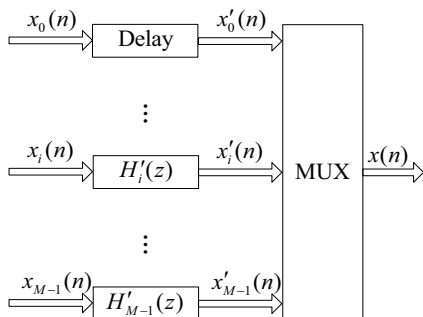


Fig. 4. Block diagram for gain and timing error correction.

There is no need to correct $x_0(n)$ for the frequency response of the reference channel calibration filter is constant, i.e. $H'_0(e^{j\omega}) = 1$, and $H'_i(e^{j\omega}), i \neq 0$ is a fractional delay filter with impulse response

$$h'_i(n) = \frac{\sin(\pi(n - \delta_i))}{(1 + g_i)\pi(n - \delta_i)}. \quad (23)$$

The impulse response in (23) is an infinite-impulse response (IIR) filter. To make the filter causal and realizable in practice with a finite-impulse response (FIR) structure [19], the $M - 1$ calibration filters $h'_i(n) (i = 1, \dots, M - 1)$ can be truncated, windowed, and delayed [9]. Any delay that is added to $h'_i(n) (i = 1, \dots, M - 1)$ must also be added to $x_0(n)$ in Fig. 4 before multiplexing to guarantee proper time alignment.

With the estimated gain and timing error parameters described in the last part, the filters in (23) can eliminate the effects of the gain and timing errors. In Fig. 4, after correction, the sample-time delay between $x'_i(n)$ and $x'_0(n)$ is iT_s .

4. Simulation results

In this section, a 4-channel 10-bit time-interleaved ADC system is designed to numerically evaluate the performance characteristics of the estimation and correction methods.

4.1. Error estimation

In practice, the ADC output will be influenced by channel noise. Assume that noise in the four channels consists of four independent zero-mean white Gaussian noises (WGNs) with the same variance, representing quantization errors and thermal noise effects, and consequently the four ADC outputs have the same signal to noise ratio (SNR). Fig. 5 shows the error estimation performance with different SNR. The gain and timing errors are $[g_0 \ g_1 \ g_2 \ g_3] = [0 \ 0.01 \ 0.02 \ -0.01]$ and $[\delta_0 \ \delta_1 \ \delta_2 \ \delta_3] = [0 \ 0.02 \ 0.01 \ -0.02]$, respectively. The DFT length for each ADC is $L = 2048$ and the input frequency is $f_0 = 0.15 f_s$. As shown in Fig. 5, the gain and timing errors can still be estimated accurately when the SNR decreases to about 20 dB for 10-bit ADC quantization.

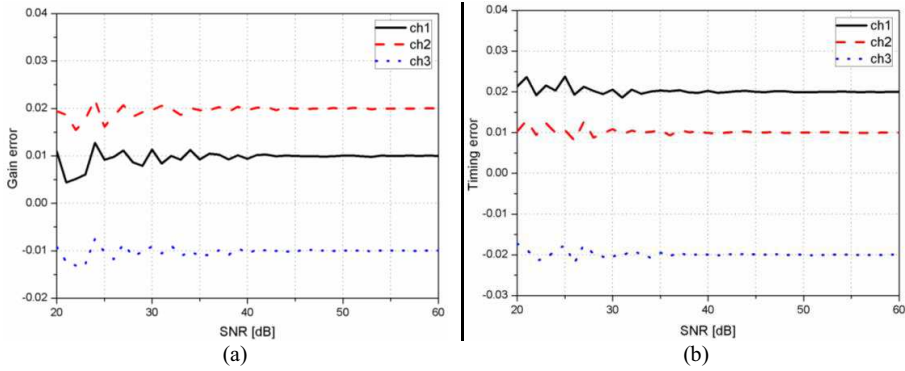


Fig. 5. Error estimates versus SNR: a) gain error. b) timing error. $[g_0 \ g_1 \ g_2 \ g_3] = [0 \ 0.01 \ 0.02 \ -0.01]$ and $[\delta_0 \ \delta_1 \ \delta_2 \ \delta_3] = [0 \ 0.02 \ 0.01 \ -0.02]$, $f_0 = 0.15 f_s$.

Fig. 6 shows the gain and timing error estimates with 100 different input frequencies. The gain and timing errors are the same as in Fig. 5. The DFT length for each ADC is also $L=2048$ and the test frequency is restricted by (16). The SNR of each channel is about 45 dB. It can be concluded from Fig. 6 that the gain and timing errors can be properly estimated with different input test frequency.

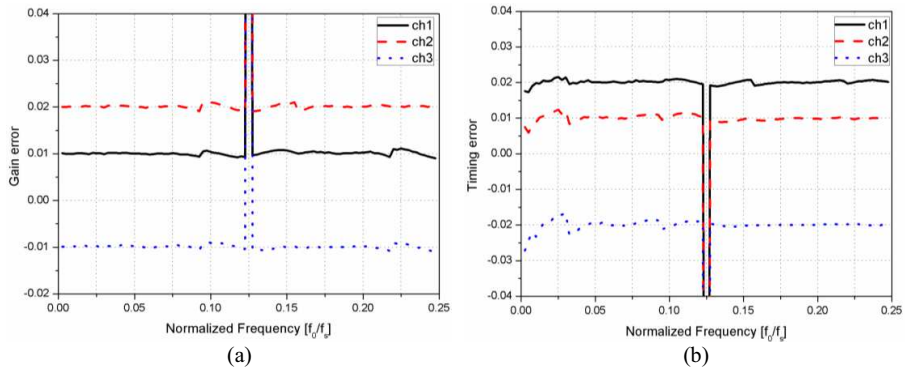


Fig. 6. Error estimates versus frequency: a) gain error, b) timing error.

4.2. Error correction

In the simulations for error correction presented here, the channel calibration filter $h'_i(n)$ is approximately implemented by 30-tap FIR filters, which is obtained by applying a Blackman window to the IIR filters $h_i(n)$ in (23).

Fig. 7 (a) shows the output spectrum of the time-interleaved ADC system with the same gain and timing error parameters as in Fig. 5. The input frequency is $f_0 = 0.07 f_s$ and the images due to the gain and timing errors appear at $f_i = 0.18 f_s, 0.32 f_s$ and $0.43 f_s$. Fig. 7 (b) shows the output spectrum with gain and timing error correction.

Fig. 8 shows spectra before and after gain and timing correction when the input consists of two equal-amplitude sinusoids at $0.05 f_s$ and $0.35 f_s$. Here, the estimates of gain and timing errors are obtained by applying a frequency lower than $0.25 f_s$ (e.g. $0.05 f_s$) to the four channels. In Fig. 8 (a), there are six images caused by the two input frequencies, and their magnitudes are much smaller after correction.

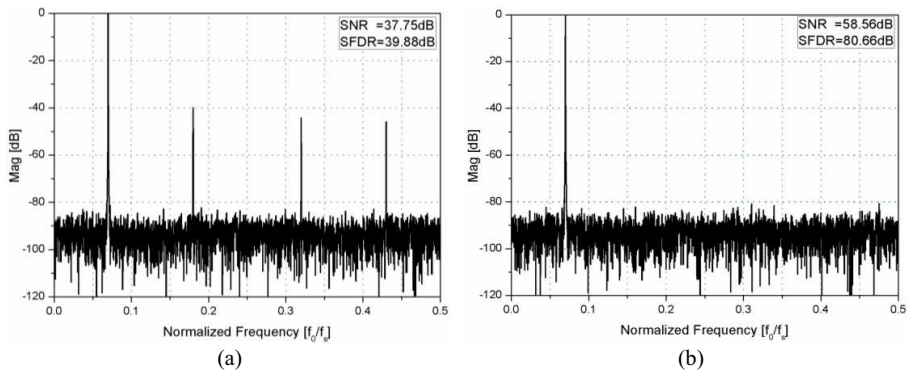


Fig. 7. The spectra of ADC output with gain and timing error: a) without and b) with correction.

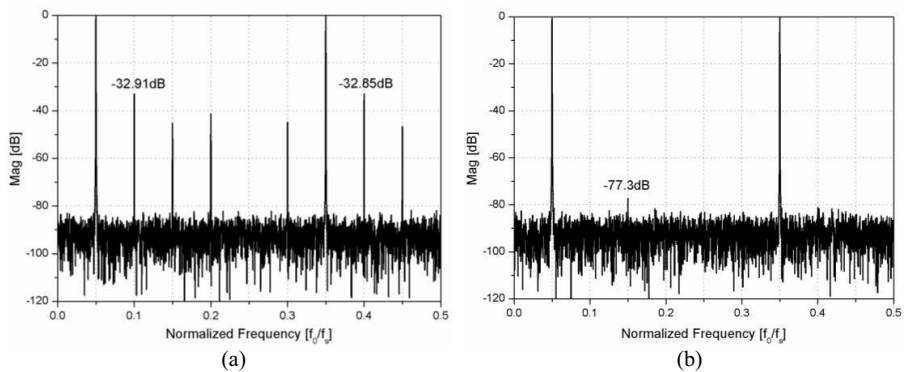


Fig. 8. ADC output spectra when the input consists of two equal-amplitude sinusoids: a) without and b) with correction.

5. Conclusions

Mismatches between the channels degrade the performance of the time-interleaved ADCs. In this paper, an algorithm based on DFT has been derived to estimate and correct the gain and timing errors. With a sinusoidal input, the estimation is achieved by using the magnitude and phase of the DFT of each ADC output, and a frequency range to ensure the proper estimation is presented. The gain and timing errors can be corrected by a set of calibration filters before the multiplexing. The estimation and correction algorithm presented in this paper can calibrate the gain and timing errors accurately, and it is simple to implement in practice.

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